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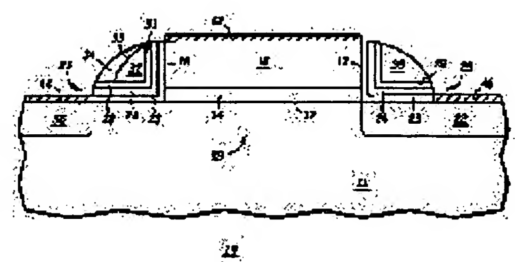
(54) SPLIT GATE MEMORY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a nonvolatile memory device excellent in power efficiency and suitable for low power application, by a method wherein electric charges carriers generated from a source of a source area range over a channel area and accelerate, and are implanted into a dielectric layer located in a floating gate or under a control gate, and a selective gate controls a channel current.
SOLUTION: A nonvolatile memory(NVM) device comprises a control gate 32 on a first portion of a channel area near a source, and split gate field-effect transistors(FET) having a selection gate 16 on a second portion of a channel area 38 near a drain. When the NVM device is programmed, electric charges carriers of a first polarity accelerate in the second portion of the channel area 38 under the selection gate 16, and are implanted into a lower dielectric layer 14 of the control gate 32. When data are read from the NVM device, a read voltage is applied to a drain adjacent to the selection gate 16 a current of a bit line coupled to the drain of FET is detected, and data are read out.



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CLAIMS

[Claim(s)]
[Claim 1] a split-gate memory apparatus -- it is -- body [of :semiconductor material]; -- source field [within said body of a semiconductor material]; -- drain field [within said body of a semiconductor material]; -- said source field is separated from said drain field -- It is the 1st conductive layer which exists on said dielectric layer. channel field [within said body of a semiconductor material]; -- dielectric layer; which exists in the top for said channel field contiguous to said drain field part I -- dielectric laminating section; which exists in the top for said channel field contiguous to said source field part II -- The split-gate memory apparatus characterized by being constituted by 2nd conductive layer; which exists on 1st conductive layer; which has the 1st side attachment wall which **** to said drain field, and the 2nd side attachment wall which counters said 1st side attachment wall, and said dielectric laminating section, and **** on said 2nd side attachment wall of said 1st conductive layer.
[Claim 2] a split-gate memory apparatus -- it is -- body [of :semiconductor material]; -- source field [within said body of a semiconductor material]; -- drain field [within said body of a semiconductor material]; -- said source field is separated from said drain field -- It is the 1st conductive layer which exists in the top for said said channel field part I. channel field [within said body of a semiconductor material]; -- dielectric layer; which exists in the top for said channel field part I -- oxide-nitride-oxide layer; which exists in the top for said channel field contiguous to said source field part II -- It is the conductive side-attachment-wall spacer which exists in the top for said 1st conductive layer; which has the 1st side attachment wall and the 2nd side attachment wall which counters said 1st side attachment wall, and said channel field part II. The amount of [of said oxide-nitride-oxide layer] part I exists between said conductive side-attachment-wall spacer and said 2nd side attachment wall of said 1st conductive layer. The split-gate memory apparatus characterized by being constituted by conductive side-attachment-wall spacer; to which the amount of [of said oxide-nitride-oxide layer] part II exists between parts for said conductive side-attachment-wall spacer and said part II of said channel field.
[Claim 3] a split-gate memory apparatus -- it is -- body [of :semiconductor material]; -- source field [within said body of a semiconductor material]; -- drain field [within said body of a semiconductor material]; -- said source field is separated from said drain field -- It is the 1st conductive layer which exists in the top for said said channel field part I. channel field [within said body of a semiconductor material]; -- dielectric layer; which exists in the top for said channel field part I -- oxide-nitride-oxide layer; which exists in the top for said channel field contiguous to said source field part II -- The 1st conductive layer which has the 1st side attachment wall and the 2nd side attachment wall which counters said 1st side attachment wall; It is the 1st conductivity side-attachment-wall spacer which exists in the top for said said channel field part II. The amount of [of said oxide-nitride-oxide layer] part I exists between said 1st conductivity side-attachment-wall spacer and said 2nd side attachment wall of said 1st conductive layer. The amount of [of said oxide-nitride-oxide layer] part II exists between parts for said 1st conductivity side-attachment-wall spacer and said part II of said channel field. The split-gate memory apparatus characterized by being constituted by 2nd conductivity side-attachment-wall spacer; which **** on said 1st side attachment wall of 1st conductivity side-attachment-wall spacer [of a place];, and said 1st conductive layer.
[Claim 4] It is a split-gate memory apparatus and is the array of the memory cell arranged by two or more trains and two or more lines on :semi-conductor substrate. Each memory cell in said array is the source field, channel field, and drain field in said semi-conductor substrate. The source field, channel field, and drain field where said channel field separates said source field from said drain field, The 1st dielectric layer which exists in the top for said channel field part I, and the 2nd dielectric layer which exists in the top for said channel field which **** to said source field part II, The control gate which exists on said 2nd dielectric layer, The array of a memory cell equipped with the selector gate which exists on said 1st dielectric layer; It sets in the 1st train among said two or more trains in said array. The 1st bit line combined with said drain field of each memory cell; It sets in the 2nd train among said two or more trains in said array. The 2nd

bit line combined with said drain field of each memory cell; It sets to the 1st line of said two or more lines in said array. The 1st selection line combined with said selector gate of each memory cell; It sets to the 2nd line of said two or more lines in said array. The 1st control line combined with said control gate of each memory cell in the aforementioned 2nd selection line; 1st line combined with said selector gate of each memory cell; 2nd control-line; combined with said control gate of each memory cell in said 2nd line, and said 1st line And the split-gate memory apparatus characterized by being constituted by source line; combined with said source field of each memory cell in said 2nd line.

[Claim 5] It is a split-gate memory apparatus and is the array of the memory cell arranged by two or more trains and two or more lines on :semi-conductor substrate. Each memory cell in said array The source field, channel field, and drain field where it is the source field, channel field, and drain field in said semi-conductor substrate, and said channel field separates said source field from said drain field, The 1st dielectric layer which exists in the top for said channel field contiguous to said drain field part I, The oxide-nitride-oxide dielectric layer which exists in the top for said channel field contiguous to said source field part II, The control gate which exists on said oxide-nitride-oxide dielectric layer, The array of a memory cell equipped with the selector gate which exists on said 1st dielectric layer; It sets in the 1st train among said two or more trains in said array. The 1st bit line combined with said drain field of each memory cell; It sets in the 2nd train among said two or more trains in said array. The 2nd bit line combined with said drain field of each memory cell; It sets to the 1st line of said two or more lines in said array. The 1st selection line combined with said selector gate of each memory cell; It sets to the 2nd line of said two or more lines in said array. The 1st control line combined with said control gate of each memory cell in the aforementioned 2nd selection line; 1st line combined with said selector gate of each memory cell; 2nd control-line; combined with said control gate of each memory cell in said 2nd line, and said 1st line And the split-gate memory apparatus characterized by being constituted by source line; combined with said source field of each memory cell in said 2nd line.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Generally this invention relates to nonvolatile memory equipment in more detail about a memory apparatus.
[0002]
[Description of the Prior Art] The programmable read only memory (EEPROM: Electrically Erasable Programmable Read Only Memory) in which an eliminable store is possible can hold electrically the data stored even if the power to memory was eliminated. An EEPROM cel accumulates a charge into the floating gate separated electrically [a field-effect transistor (FET: field effect transistor)], or is FET. Data are stored by accumulating a charge into the dielectric layer under the control gate. The stored charge is FET. A threshold is controlled and this controls the memory condition of an EEPROM cel.
[0003] Conventionally, an EEPROM cel pours in a charge carrier using drain side hot carrier impregnation into the charge trap site in the dielectric layer on the floating gate or under the control gate. A programming process is accelerated using a high drain and gate voltage. For this reason, FET in an EEPROM cel Although a high current is told during programming, this is not desirable in the application of low-battery low power. Furthermore, an EEPROM cel operates in the condition very near a breakdown condition during programming.
[0004] The yield condition under programming is avoidable if source side carrier injection is used. In order to program EEPROM using source side hot carrier impregnation, a selector gate is formed on [some] the channel field contiguous to a source field. This selector gate is electrically separated from the control gate adjoined and formed in a drain field. During programming, electric field are set up in a channel field, and the charge carrier which emits a source to a source field by that cause is poured in into the dielectric layer located in the floating gate and under the control gate, after continuing a channel field and being accelerated. A selector gate controls channel current. In this way, compared with the conventional drain side hot carrier impregnation, programming by source side hot carrier impregnation is excellent in power efficiency, and suitable with the low-battery low power application.
[0005] Therefore, it is advantageous to have the nonvolatile memory equipment which was excellent in power efficiency and fitted the low power application, and the approach of accessing nonvolatile memory equipment. Moreover, this nonvolatile memory equipment is easy to manufacture, a cheap thing is desirable and it is desirable for silicon area effectiveness to be good. Furthermore, as for this access approach, it is desirable for it to be reliable and to excel in time amount effectiveness.
[0006]
[Example] Generally, this invention offers nonvolatile memory (NVM: nonvolatile memory) equipment and the approach of accessing NVM **. By this invention, it is NVM. Equipment is equipped with the split-gate field-effect transistor (FET) which has the control gate which exists in the top for the channel field near the source part I, and the selector gate which exists in the top for the channel field near a drain part II. NVM In case equipment is programmed, it is accelerated within the part II part of the channel field under a selector gate, and the electronic charge carrier of the 1st polarity is poured in into the dielectric layer which exists under the control gate. In the suitable example of this invention, the dielectric layer which exists under the control gate is constituted by the pars-basilaris-ossis-occipitalis dielectric layer (for example, pars-basilaris-ossis-occipitalis diacid-ized silicon layer) on the part I part of a channel field, the up dielectric layer (for example, up diacid-ized silicon layer) under the control gate, and the silicon nitride layer among them. A silicon nitride layer includes the charge trap site (charge trapping site) formed into it. NVM Equipment is eliminated by pouring in the charge carrier of the 2nd polarity of an electron hole etc. into a silicon nitride layer from a channel field. NVM When reading data in equipment, a read electrical potential difference adjoins a

selector gate, and drain impression is carried out. Next, FET By detecting the current which flows the bit line combined with a drain, data are NVM. It is read in equipment.
[0007] Drawing 1 is NVM by this invention. It is the sectional view of split-gate memory apparatus, such as a cel 10. NVM A cel 10 is formed on the body of semiconductor materials, such as the semi-conductor substrate 11 which has the main front face 12. As an example, the semi-conductor substrate 11 is p. It is the silicon substrate of a conductivity type. It is NVM so that it may be explained below. A store (programming) and elimination are electrically possible for a cel 10. Therefore, NVM A cel 10 is also electrically called the programmable read only memory (EEPROM: Electrically Erasable Programmable ReadOnly Memory) cel in which an elimination store is possible.
[0008] The selector-gate structure 15 is equipped with the selector gate 16 on the dielectric layer 14 and dielectric layer 14 which exist on a substrate 11. A selector gate 16 has the side attachment walls 17 and 18 which counter mutually. As an example, a dielectric layer 14 is a heat growth diacid-ized silicon layer which has the thickness of about 3 nanometers (nm) thru/or about 30nm, and a selector gate 16 is formed deposition and by carrying out patterning in a conductive layer on a dielectric layer 14. Preferably, a conductive layer is a polycrystalline silicon layer which has the thickness of about 150nm thru/or about 300nm, and deposition is carried out on a dielectric layer 14 using a chemical-vacuum-deposition process. Furthermore, a selector gate 16 is n between a chemical-vacuum-deposition process or a subsequent doping phase. It is desirable to be doped with the ion of a conductivity type, for example, Lynn, or arsenic ion.
[0009] The drain field 22 is adjusted with the side attachment wall 17 of a selector gate 16. As an example, they are n, such as Lynn or arsenic ion. The drain field 22 is formed using the self-align ion-implantation process of pouring in the ion of a conductivity type into a substrate 11. Preferably, an ion-implantation process penetrates the pad dielectric layer on the main front face 12 of a substrate 11, and is performed. A dielectric layer 14, a sacrifice oxide layer (not shown), etc. are sufficient as a pad dielectric layer.
[0010] For example, dielectric layers, such as the diacid-ized silicon layer 23, are formed on the part on the front face 12 of main contiguous to the side attachment walls 17 and 18 of a selector gate 16. Preferably, the diacid-ized silicon layer 23 has the thickness of about 5nm thru/or about 15nm, and is formed using a thermal oxidation process or a deposition process. Since a thermal oxidation process also oxidizes a selector gate 16 in accordance with side attachment walls 17 and 18, even if the diacid-ized silicon layer 23 meets side attachment walls 17 and 18, it is formed. In a certain example, etching clearance of the part of the dielectric layer 14 which is not protected by the selector gate 16 is carried out, and the diacid-ized silicon layer 23 is formed on the main front face 12 after that. In other examples, the diacid-ized silicon layer 23 is formed on the part of the dielectric layer 14 which is not protected by the selector gate 16. For example, the silicon nitride layer 24 which has the thickness of about 5nm thru/or about 15nm is formed on the diacid-ized silicon layer 23, and is preferably formed using a chemical-vacuum-deposition process. For example, another dielectric layers, such as the diacid-ized silicon layer 28 which has the thickness of about 5nm thru/or about 15nm, are formed on the silicon nitride layer 24. The diacid-ized silicon layer 28 can be formed using a deposition process or a thermal oxidation process.
[0011] The diacid-ized silicon layer 23, the silicon nitride layer 24, and the diacid-ized silicon layer 28 form the oxide-nitride-oxide (ONO: oxide-nitride-oxide) laminating section 25. This is also called the dielectric laminating section. ONO In the laminating section 25, the diacid-ized silicon layer 23 is called a pars-basilaris-ossis-occipitalis dielectric layer, and the diacid-ized silicon layer 28 is called an up dielectric layer. NVM In case a cel 10 is programmed, a charge carrier (for example, electron) is ONO. It is poured in into the laminating section 25 and caught in the charge trap site formed in the silicon nitride layer 24. NVM In order for a cel 10 to have a good rate of data-hold, it is desirable that the pars-basilaris-ossis-occipitalis dielectric layer 23 and the up dielectric layer 28 are thick. Furthermore, it is desirable to suppress the defect in a dielectric layer 23 and 28 to the minimum. The chemical composition of the silicon nitride layer 24 is Si_3N_4. Please understand not restricting. For example, the silicon nitride layer 24 can be used as the nitride layer which was rich in the silicon which has the chemical composition expressed with Si_xN_y. However, x Pair y A ratio is larger than 3 to 4.
[0012] The control gate 32 is ONO. It exists on the laminating section 25. The control gate 32 has the side attachment wall 31 which adjoins a selector gate 16, and the side attachment wall 33 which counters a side attachment wall 31. As an example, the control gate 32 is ONO. A conductive layer is formed deposition and by carrying out patterning on the laminating section 25. Preferably, a conductive layer is a polycrystalline silicon layer which has the thickness of about 200nm thru/or about 300nm, and deposition is carried out on the ONO laminating section 25 using a chemical-vacuum-deposition process. As for the control gate 32, in other words, it is desirable to be formed as a polycrystalline silicon side-attachment-wall spacer which adjoins a selector gate 16. Furthermore, the control gate 32 is n, such as Lynn or arsenic ion. It is conductivity-type ion and it is desirable to be doped between chemical-vacuum-deposition processes or

between subsequent doping phases. The process which forms the control gate 32 also forms a polycrystalline silicon side-attachment-wall spacer (not shown) in accordance with the side attachment wall 17 of a selector gate 16. However, the polycrystalline silicon side-attachment-wall spacer in alignment with the side attachment wall 17 of a selector gate 16 is NVM. It does not participate in actuation of a cel 10. It is NVM which this is removed all over a subsequent etching phase in a certain example, and is illustrated by drawing 1 . It becomes a cel 10. It sets in the another example (not shown) and this spacer is NVM. It is combined by reference voltage levels, such as a touch-down voltage level, during the access actuation to a cel 10.

[0013] Respectively in accordance with the side attachment wall 33 of the control gate 32, and the side attachment wall 17 of a selector gate 16, dielectric spacers, such as the nitride spacers 34 and 35, are formed. Preferably, the nitride spacer 34 is a wrap about the control gate 32. The source field 36 is adjusted with the nitride spacer 34. As an example, they are n, such as Lynn or arsenic ion. The source field 36 is formed using the self-align ion-implantation process of pouring in the ion of a conductivity type. The source field 36 and the drain field 22 specify the channel field 38 among them. In other words, the channel field 38 separates the source field 36 from the drain field 22. A part for part I of the channel field 38 is ONO. Being under the laminating section 25 and the control gate 32, the amount of [of the channel field 38] part II is under the selector-gate structure 15. The nitride spacers 34 and 35 are NVM. Please understand arbitrary things in a cel 10. NVM In the example of the alternative in which a cel 10 does not contain the nitride spacers 34 and 35, the source field 36 is adjusted with the side attachment wall 33 of the control gate 32.

[0014] ONO By the process which forms the laminating section 25 on the main front face 12, it is ONO also on a selector gate 16. The laminating section is formed (not shown). ONO in the selector-gate 16 upper part The parts (not shown) of the laminating section and the ONO layer 25 which is on the main front face 12 and is not protected by the nitride spacers 34 and 35 are removed in an etching process. The silicon compound structure 42 exists on a selector gate 16, and it is NVM. It functions as a selector-gate electrode of a cel 10. Similarly, the silicon compound structure 44 exists on the source field 36, and it is NVM. It functions as a source electrode of a cel 10. Furthermore, the silicon compound structure 46 exists on the drain field 22, and it is NVM. It functions as a drain electrode of a cel 10. The silicon compound structures 42, 44, and 46 are adjusted with the nitride spacers 34 and 35. For this reason, these are also called self-align silicon compound (Salicide) structure. The silicon compound structures 42, 44, and 46 are NVM. Since the parasitism resistance in a cel 10 is mitigated, it is NVM. The engine performance of a cel 10 is improved. However, the silicon compound structures 42, 44, and 46 are NVM. Please care about that it is the component of arbitration in a cel 10.

[0015] Flattening of the insulating layer (not shown) is formed and carried out on a substrate 11 after formation of the silicon compound structures 42, 44, and 46. A metallic-coating field (not shown) is formed in an insulating layer, and it is electrically combined with the control gate 32, the selector-gate electrode 42, the source electrode 44, and the drain electrode 46.

[0016] Although it is shown that drawing 1 is formed as a side-attachment-wall spacer which the control gate 32 **** to a selector gate 16, this does not restrict this invention. In the example of an alternative of this invention, a polycrystalline silicon selector gate is formed as a side-attachment-wall spacer along the polycrystalline silicon control gate. It sets to this example and the 1st polycrystalline silicon layer is ONO. Patterning is carried out on the laminating section 25, and the control gate is specified. ONO to which the control gate does not exist upwards Etching clearance of the part of the laminating section 25 is carried out. A dielectric layer 14 is arranged on the main front face 12. An ion implantation is performed and the control gate and the source field 36 adjusted are formed. Deposition of the 2nd polycrystalline silicon layer is carried out on a dielectric layer 14, and patterning is carried out so that a selector gate may be formed as a side-attachment-wall spacer of the control gate. An ion implantation is performed once again and forms a selector gate and the drain field 22 adjusted.

[0017] it is mentioned above -- as -- NVM a cel 10 -- p n created in the conductivity-type substrate 11 Channel split gate FET it is . However, this does not restrain this invention. a substitute example -- setting -- NVM a cel 10 -- n p created in a conductivity-type semi-conductor substrate Channel split gate FET it is . another example -- setting -- NVM a cel 10 -- n p formed in a conductivity-type semi-conductor substrate n created in the well of a conductivity type Channel split gate FET it is . still more nearly another example -- setting -- NVM a cel 10 -- p n formed in a conductivity-type semi-conductor substrate p created in the well of a conductivity type Channel split gate FET it is .

[0018] NVM of drawing 1 Access to a cel 10 is : containing three parts, i.e., NVM. Programming a cel 10 and NVM Eliminating a cel 10 and NVM It is reading data in RU 10. These are NVM. It realizes by carrying out bias of the selector gate 16, the control gate 32, the source field 36, and the drain field 22 of a cel 10 to a predetermined electrical potential difference.

[0019] NVM In order to program a cel 10 electrically, programming drain electrical potential differences, such as a

touch-down electrical potential difference, are impressed to the drain field 22. At least, the programming selector-gate electrical potential difference by threshold voltage of channel field 38 part under the selector-gate structure 15 higher than a programming drain electrical potential difference is impressed to a selector gate 16. A programming source electrical potential difference higher than a programming drain electrical potential difference is impressed to the source field 36. Furthermore, programming control gate voltage higher than a programming source electrical potential difference is impressed to the control gate 32. As an example, about 1 volt thru/or about 2 volts, and the programming source electrical potential difference of a programming selector-gate electrical potential difference are about 3 volts thru/or about 5 volts, and programming control gate voltage is about 8 volts thru/or about 10 volts.

[0020] Since it is in a voltage level higher than the drain field 22, the source field 36 is n. Channel split-gate FET 10 operate in reversal active mode. In other words, during programming, the source field 36 functions as a drain of FET 10, and the drain field 22 functions as the source of FET 10. Furthermore, a selector gate 16 is in the voltage level [at least] by threshold voltage of channel field 38 part under the selector-gate structure 15 higher than the voltage level of the drain field 22. For this reason, the part of the channel field 38 under the selector-gate structure 15 is turned on, and has conductivity. A negative charge carrier, for example, an electron, is generated from the drain field 22, and it is accelerated through channel field 38 part between the selector-gate structure 15 and the control gate 32. a charge carrier -- the source field 36 -- adjoining -- in addition -- and it will be drawn by the high tension in the control gate 32 if channel field 38 part under the control gate 32 is reached. In a hot carrier impregnation process, a charge carrier is poured in through an oxide layer 23, and it is caught in the part of the silicon nitride layer 24 which **** on the side attachment wall 31 of the control gate 32. The threshold voltage of channel field 38 part under the control gate 32 goes up as a negative charge carrier, for example, an electron, moves into the silicon nitride layer 24 from the channel field 38. For this reason, the current passing through the channel field 38 falls, and the rate of hot carrier impregnation also falls. NVM After a programming electrical potential difference is eliminated from a cel 10, the poured-in carrier becomes with the condition of having been caught in the silicon nitride layer 24. The 1st logical value 1, for example, logic, is NVM. It is stored in a cel 10. Namely, NVM A cel 10 is programmed.

[0021] The current which flows the channel field 38 is restricted between programming processes by the programming selector-gate voltage level impressed to a selector gate 16. Preferably, a programming selector-gate electrical potential difference is somewhat higher than the threshold voltage of channel field 38 part under a selector gate 16, and the current which flows the inside of the channel field 38 by that cause is suppressed to the minimum. In this way, it is NVM. The process which programs a cel 10 is excellent in power efficiency, and suitable for a low-battery low power application.

[0022] NVM In order to eliminate a cel 10 electrically, an elimination source electrical potential difference is impressed to the source field 36, and elimination control gate voltage lower than an elimination source electrical potential difference is impressed to the control gate 32. As an example, elimination source electrical potential differences are about 5 volts thru/or about 7 volts, and elimination control gate voltage is [about]. -It is [about / 11 volts thru/or]. -It is 9 volts. It does not participate in an elimination process, but is combined with a reference voltage level, for example, a touch-down voltage level, or a selector gate 16 and the drain field 22 can be made into floating. NVM In the example of the alternative which eliminates a cel 10, an elimination selector-gate electrical potential difference is impressed to a selector gate 16, and an elimination drain electrical potential difference is impressed to the drain field 22. At this time, an elimination selector-gate electrical potential difference is lower than an elimination drain electrical potential difference. As an example, an elimination selector-gate electrical potential difference is [about]. -It is [about / 3 volts thru/or]. -It is 0.5 volts and an elimination drain electrical potential difference is a touch-down electrical potential difference. Since a selector gate 16 is in a voltage level lower than the drain field 22, channel field 38 part under a selector gate 16 certainly has non-conductive. NVM The electrical potential difference of about 2 volts thru/or about 5 volts is impressed to the drain field 22, and it is made for charge carrier injection not to happen from the drain field 22 to the channel field 38 accidentally in another alternative example which eliminates a cel 10.

[0023] In the channel field 38 part under the control gate 32, powerful electric field are set up a sake [between the source field 36 and the control gate 32 (for example a high-tension difference (about 14 volts thru/or about 19 volts))]. According to a band tunnel process, strong electric field generate an electronic-electron hole pair within the channel field 38 part which adjoins the source field 36. The electron hole which is a positive charge carrier is drawn by the negative electrical potential difference at the control gate 32. In a hot carrier impregnation process, an electron hole minds an oxide layer 23, and it is ONO. It is poured in to the silicon nitride layer 24 of the laminating section 25, and combines with the electron in the silicon nitride layer 24 there. Preferably, an elimination process continues until the silicon nitride layer 24 is substantially charged by electrical neutrality or forward. Blanking voltage is NVM. If removed from a cel 10, the silicon nitride layer 24 will become with neutrality or the condition of having just charged,

substantially. In any case, the 2nd logical value 0, for example, logic, is NVM. It is stored in a cel 10. Namely, NVM A cel 10 is eliminated.

[0024] The charge with which it is stored in the charge trap site of the silicon nitride layer 24 between elimination processes is carbonated with the charge of antipole nature poured in from the channel field 38. The charge in a charge trap site is Fowler-Nordheim. As compared with the elimination process which moves to the control gate through a dielectric layer in a tunnel process between a charge trap site and the control gate, it is ONO in the elimination process of this invention. The up dielectric layer 28 thick in the laminating section 25 becomes possible, and, thereby, it is NVM. The data-hold of a cel 10 is improved.

[0025] NVM In order to read data in a cel 10, reading source electrical potential differences, such as a touch-down electrical potential difference, are impressed to the source field 36. It is substantially [as a reading source electrical potential difference] equal, or reading control gate voltage higher than it is impressed to the control gate 32. At least, the reading selector-gate electrical potential difference by threshold voltage of channel field 38 part under the selector-gate structure 15 higher than a reading source electrical potential difference is impressed to a selector gate 16. In this way, channel field 38 part under the selector-gate structure 15 is turned on, and has conductivity. A reading drain electrical potential difference higher than a reading source electrical potential difference is impressed to the drain field 22. As an example, about 1 volt thru/or about 2 volts, and the reading drain electrical potential difference of reading control gate voltage are about 1 volt thru/or about 2 volts, and a selector gate 16 is supply voltage VDD. It is combined. As an example, it is supply voltage VDD. They are about 3 volts thru/or about 5 volts. It sets for a low power application and is supply voltage VDD. For example, they are about 0.9 volts thru/or about 1.8 volts.

[0026] NVM If a cel 10 is programmed, the silicon nitride layer 24 under the control gate 32 will be charged by negative. Channel field 38 part under the control gate 32 has threshold voltage with the silicon nitride layer 24 substantially higher than the proper threshold voltage at the time of electrical neutrality under the control gate 32. NVM If a cel 10 is eliminated, the silicon nitride layer 24 under the control gate 32 will become electrical neutrality substantially, or will just be charged. Channel field 38 part under the control gate 32 is substantially [as the proper threshold voltage] equal, or has threshold voltage lower than it. Reading control gate voltage is NVM. When a cel 10 is programmed, it is desirable that it is lower than the threshold voltage of channel field 38 part under the control gate 32. Moreover, reading control gate voltage is NVM. When a cel 10 is eliminated, it is desirable that it is higher than the threshold voltage of channel field 38 part under the control gate 32. Therefore, programmed NVM When reading data in a cel 10, the current of the channel field 38 which serves as non-conductive and flows that is as small as for example, below about 2microampere (muA). The detection amplifier (not shown) combined with the drain field 22 through a bit line (not shown to drawing 1) detects this small current, and is NVM. The 1st logical value 1, for example, logic, is read in a cel 10. NVM eliminated on the other hand The current which the channel field 38 has conductivity and flows that when reading data in a cel 10 is about 10microA. It becomes large with the above. The detection amplifier (not shown) combined with the drain field 22 detects this big current, and is NVM in the 2nd logical value 0, for example, logic. It reads in a cel 10.

[0027] The source field 36 is in a voltage level lower than the drain field 22 between the processes to read. The voltage drop covering channel field 38 part under the control gate 32 is small. For this reason, the probability for a charge carrier to be accidentally poured in into the silicon nitride layer 24 from the channel field 38 is small. In other words, it is NVM. The active jamming in a reading process over the data stored in a cel 10 is small. A detection amplifier (not shown) is combined with the drain field 22 through a bit line (not shown to drawing 1) by this invention, and the drain field 22 is separated from the silicon nitride layer 24 by the selector-gate structure 15 by it. Therefore, the capacity of a parasitism bit line capacitor is substantially unrelated to the charge in the silicon nitride layer 24. In other words, the data dependency of parasitism bit line capacity is NVM. In a cel 10, it is small. NVM NVM with the small data dependencies of bit line capacity, such as a cel 10, RU is suitable for a high performance application.

[0028] Drawing 2 is the split gate NVM by this invention. It is the wiring schematic of equipment 50. NVM Equipment 50 is the split gate FET which was created in the semi-conductor substrate (not shown to drawing 2), and was arranged by the line and the train. It has an array. Split gate FET NVM In equipment 50, it functions as a memory cell. Each split gate FET in an array It has a source field, a drain field, and the channel field that separates a source field from a channel field. Selector-gate structure exists on the channel field part which adjoins a drain field. The dielectric laminating section exists on another part of the channel field contiguous to a source field. The control gate is arranged on the dielectric laminating section, and it insulates from a selector gate electrically. Split gate FET in an array 1-bit data are stored. Therefore, split gate FET in an array NVM In equipment 50, it is also called a bit cel. Preferably, it is NVM. Split gate FET in equipment 50 Split gate NVM illustrated by drawing 1 It is structurally [as a cel 10] equal. Drawing 2 shows 16 bit cels arranged by four-line four trains. However, this does not restrain this invention. By this invention, it

is NVM. Equipment 50 is equipped with the array of the bit cel arranged by the line of the number of arbitration, and the train of the number of arbitration.
[0029] NVM Equipment 50 is accessed through the source lines 52 and 54, the selection lines 61, 62, 63, and 64, the control lines 71, 72, 73, and 74, and bit lines 81, 82, 83, and 84. NVM The bit cel in equipment 50 is addressed with the location, for example, the line number, and row number in an array. In the 1st line, the bit cel 110,120,130,140 is located in the 1st, 2nd, 3rd, and 4th trains, respectively. In the 2nd line, the bit cel 210,220,230,240 is located in the 1st, 2nd, 3rd, and 4th trains, respectively. In the 3rd line, the bit cel 310,320,330,340 is located in the 1st, 2nd, 3rd, and 4th trains, respectively. In the 4th line, the bit cel 410,420,430,440 is located in the 1st, 2nd, 3rd, and 4th trains, respectively.
[0030] The source line 52 is connected to the source 112,122,132,142 of the bit cel 110,120,130,140 of the 1st line, respectively. The source line 52 is connected also to the source 212,222,232,242 of the bit cel 210,220,230,240 of the 2nd line, respectively. The source line 54 is connected to the source 312,322,332,342 of the bit cel 310,320,330,340 of the 3rd line, respectively. The source line 54 is connected also to the source 412,422,432,442 of the bit cel 410,420,430,440 of the 4th line, respectively. Since the bit cel which combines the source with the same source line is put in block by this invention and it is eliminated, an elimination block is formed. For this reason, NVM Although equipment 50 consists of what consists of bit cels in the 1st and the 2nd line, and a bit cel in the 3rd and the 4th line, it is equipped with two elimination blocks.
[0031] The selection line 61 is connected to the selector gate 115,125,135,145 of the bit cel 110,120,130,140 of the 1st line, respectively. The selection line 62 is connected to the selector gate 215,225,235,245 of the bit cel 210,220,230,240 of the 2nd line, respectively. The selection line 63 is connected to the selector gate 315,325,335,345 of the bit cel 310,320,330,340 of the 3rd line, respectively. The selection line 64 is connected to the selector gate 415,425,435,445 of the bit cel 410,420,430,440 of the 4th line, respectively.
[0032] The control line 71 is connected to the control gate 116,126,136,146 of the bit cel 110,120,130,140 of the 1st line, respectively. The control line 72 is connected to the control gate 216,226,236,246 of the bit cel 210,220,230,240 of the 2nd line, respectively. The control line 73 is connected to the control gate 316,326,336,346 of the bit cel 310,320,330,340 of the 3rd line, respectively. The control line 74 is connected to the control gate 416,426,436,446 of the bit cel 410,420,430,440 of the 4th line, respectively.
[0033] A bit line 81 is connected to the drain 114,214,314,414 of the bit cel 110,210,310,410 of the 1st train, respectively. A bit line 82 is connected to the drain 124,224,324,424 of the bit cel 120,220,320,420 of the 2nd train, respectively. A bit line 83 is connected to the drain 134,234,334,434 of the bit cel 130,230,330,430 of the 3rd train, respectively. A bit line 84 is connected to the drain 144,244,344,444 of the bit cel 140,240,340,440 of the 4th train, respectively.
[0034] NVM Please understand that the bit cel in equipment 50 is not necessarily combined as explained above. For example, the source line 52 and the source line 54 are mutually combinable. In other words, all the sources of the 1st in an array, the 2nd, the 3rd, and the bit cel of the 4th line are combinable with the same source line. In this way, it is NVM. Equipment 50 has the elimination block constituted by the 1st, the 2nd, the 3rd, and the bit cel of the 4th line. Furthermore the control lines 71 and 72 of each other can be combined, and the control lines 73 and 74 of each other can also be combined. In this way, the bit cel in the 1st and the 2nd line shares the one control line, and the bit cel in the 3rd and the 4th line shares the one control line.
[0035] NVM Each bit cel in equipment 50 is electrically programmable according to an individual. It can read according to an individual by detecting the current on which the data stored in each bit cel also flow the inside of bit lines 81, 82, and 83 or 84. Furthermore, the bit cel within an elimination block can share and bundle up a common source line, and can eliminate it electrically. Therefore, NVM Equipment 50 is also called flash EEPROM equipment.
[0036] NVM In order to program electrically, the bit cel 110,120, for example, the bit cel, in equipment 50, the source programming electrical potential difference of about 3 volts thru/or about 5 volts is impressed to the source line 52. For example, the 1st selection programming electrical potential difference of about 1 volt thru/or about 2 volts is impressed to the selection line 61. Since the 2nd, the 3rd, and the bit cel of the 4th line do not participate in the process which programs the bit cel 110,120, they become off by impressing the 2nd selection programming electrical potential differences, such as a touch-down electrical potential difference, to the selection lines 62, 63, and 64, for example. For example, the control programming electrical potential difference of about 8 volts thru/or about 10 volts is impressed to the control line 71. Preferably, a control programming electrical potential difference is higher than a source programming electrical potential difference, and is set up more highly than the 1st selection programming electrical potential difference. The 1st bit programming electrical potential difference VDD, for example, supply voltage, It is impressed by bit lines 83 and 84. as for the difference of the 1st bit programming electrical potential difference

impressed to bit lines 83 and 84, and the 1st selection programming electrical potential difference impressed to the selection line 61, it is desirable that it is lower than the threshold voltage of the channel field part under each of the selector gate 135,145 of the bit cel 130,140. For example, the 2nd bit programming electrical potential differences, such as a touch-down electrical potential difference, are impressed to bit lines 81 and 82. Therefore, the bit cel 110,120 serves as ON and it operates in reversal active mode. In other words, the source 112,122 functions as a drain of the bit cel 110,120 between programming processes, respectively, and a drain 114,124 functions as the source of the bit cel 110,120, respectively. A negative charge carrier, for example, an electron, is generated from the drain 114,124 of the bit cel 110,120, respectively, and it is accelerated through the channel field between the selector gate 115 of the bit cel 110, and the control gate 116, and the channel field between the selector gate 125 of the bit cel 120, and the control gate 126. If a charge carrier reaches the channel field part under the control gate 116,126 of the bit cel 110,120, respectively, it will be drawn by high tension at the control gate 116,126. In a hot carrier impregnation process, a charge carrier is poured in into the charge trap site of the dielectric laminating circles under the control gate 116,126. If negative charge carriers, such as an electron, are poured in into the charge trap site under the control gate 116,126, the threshold voltage of the channel field part under the control gate 116,126 will go up. The current which flows the bit cel 110,120 falls in this way, and the rate of hot carrier impregnation also falls. NVM After a programming electrical potential difference is removed from equipment 50, the poured-in carrier remains in the charge trap site under the control gate 116,126. The 1st logical value 1, for example, logic, is stored in the bit cel 110,120. That is, the bit cel 110,120 is programmed.
[0037] NVM In order to eliminate electrically the bit cel in the bit cel of equipment 50, for example, the 1st, and the 2nd line, source blanking voltage is impressed to the source line 52, and control blanking voltage is impressed to the control lines 71 and 72. As an example, the forward electrical potential difference of about 5 volts thru/or about 7 volts is chosen as source blanking voltage, and it is [about]. -About [11 volts thru/or] -The negative electrical potential difference of 9 volts is chosen as control blanking voltage. The source line 54, the selection lines 63 and 64, and the control lines 73 and 74 are combined with a touch-down voltage level. In a certain example, the selection lines 61 and 62 and bit lines 81, 82, 83, and 84 are combined with a touch-down voltage level. In a substitute example, the selection lines 61 and 62 and bit lines 81, 82, 83, and 84 float. It sets in the another alternative example and is [about], for example. -About [3 volts thru/or] -Selection blanking voltage, such as 0.5 etc. volts, is impressed to the selection lines 61 and 62, for example, bit blanking voltage, such as a touch-down electrical potential difference, is impressed to bit lines 81, 82, 83, and 84. Since the selector gate of the bit cel of the 1st line and the 2nd line is in a voltage level lower than each drain, the channel field of the bit cel of the 1st line and the 2nd line becomes off certainly. In still more nearly another alternative example, bit blanking voltage, such as an electrical potential difference of about 2 volts thru/or about 5 volts, is impressed to bit lines 81, 82, 83, and 84, for example, and it avoids that a charge carrier is accidentally poured into the channel field of the bit cel of the 1st line and the 2nd line from a drain.
[0038] To the bottom of the 1st and the control gate near the source of a bit cel of the 2nd line, powerful electric field are set a sake [between the source of the 1st and the bit cel of the 2nd line, and the control gate (for example, a high-tension difference (about 14 volts thru/or about 18 volts))]. By the tunneling between bands, strong electric field generate an electronic-electron hole pair in the channel field part under the control gate. The electron hole which is a positive charge carrier is drawn by the negative electrical potential difference at the control gate. In a hot carrier impregnation process, an electron hole is poured in into the charge trap site of the dielectric laminating circles under each control gate. The poured-in electron hole is combined with an electron in the 1st and the charge trap site of a bit cel of the 2nd line. Preferably, an elimination process continues until the charge trap site of the 1st and the bit cel of the 2nd line becomes electrical neutrality substantially. A charge trap site may just be charged in a fault elimination process. Blanking voltage is NVM. If removed from equipment 50, the charge trap site of the 1st and the bit cel of the 2nd line will become with neutrality or the condition of having just charged, substantially. In any case, the 2nd logical value 0, for example, logic, is stored in the bit cels 110, 120, 130, and 140 and 210,220,230,240. Namely, NVM The 1st and the bit cel of the 2nd line of equipment 50 are eliminated.
[0039] NVM In order to read data in the bit cel 430,440, for example, the bit cel, of equipment 50, the 1st selection reading electrical potential difference is impressed to the selection line 64. as an example -- the 1st selection reading electrical potential difference -- supply voltage VDD it is . For example, the control reading electrical potential difference of about 1 volt thru/or about 2 volts is impressed to the control line 74. Since the bit cel in the 1st, the 2nd, and the 3rd line does not participate in the reading process of the data from the bit cel 430,440, it is desirable by impressing the 2nd selection reading electrical potential differences, such as a touch-down electrical potential difference, to the selection lines 61, 62, 63, and 64, for example to turn OFF. A source reading electrical potential difference, for example, a touch-down electrical potential difference, is impressed to the source lines 52 and 54. The 1st bit reading electrical potential difference of about 1 volt thru/or about 2 volts is impressed to bit lines 83 and 84.

Preferably, the 2nd bit reading electrical potential difference impressed to bit lines 81 and 82 is substantially [as the source reading electrical potential difference impressed to the source lines 52 and 54] equal. It becomes zero substantially between the processes in which the current which flows the inside of the bit cel 410,420 reads data in the bit cel 430,440 in this way. The control reading electrical potential difference impressed to the control line 74 is the height of extent preferably same at least as the source reading electrical potential difference impressed to the source line 54. the source reading electrical potential difference desirable [which is impressed to the selection line 64 / 1st selection reading] and impressed to the source line 54 -- at least -- the selector gate 435,445 of the bit cel 430,440 -- it is high by the threshold voltage of the channel field part under each. The 2nd selection reading electrical potential difference impressed to the selection lines 61, 62, and 63 is lower than the sum of the threshold voltage of the channel field part under the 1st, the 2nd, or the selector gate of a bit cel of the 3rd line, and the source reading electrical potential difference impressed to the source lines 52 and 54 preferably.

[0040] If the bit cel 430 is programmed, the charge trap site under the control gate 436 will be charged by negative. The channel field part under the control gate 436 has threshold voltage higher than the proper threshold voltage substantially [a charge trap site] at the time of electrical neutrality. If the bit cel 430 is eliminated, the charge trap site under the control gate 436 will be substantially charged by electrical neutrality or forward. The channel field part under the control gate 436 is substantially [as the proper threshold voltage] equal, or has threshold voltage lower than it. Preferably, the control reading electrical potential difference impressed to the control line 74 is lower than the threshold voltage of the channel field part under the control gate 436, when the bit cel 430 is programmed, and when the bit cel 430 is eliminated, it is higher than the threshold voltage of the channel field part under the control gate 436. Therefore, the current which the channel field of the bit cel 430 is non-conductive, and flows that in case data are read in the programmed bit cel 430 is about 2microA. It is as small as the following. The detection amplifier (not shown) combined with a bit line 83 detects this small current, and the 1st logical value 1, for example, logic, is read in the bit cel 430. The current which the channel field of the bit cel 430 has conductivity, and flows that on the other hand in case data are read in the eliminated bit cel 430 is about 10microA. It is as large as the above. The detection amplifier (not shown) combined with a bit line 83 detects this high current, and reads the 2nd logical value and logic 0 in the bit cel 430.

[0041] If the bit cel 440 is programmed, the charge trap site under the control gate 446 will be charged by negative. The channel field part under the control gate 446 has threshold voltage higher than the proper threshold voltage substantially [a charge trap site] at the time of electrical neutrality. If the bit cel 440 is eliminated, the charge trap site under the control gate 446 will be substantially charged by electrical neutrality or forward. The channel field part under the control gate 446 is substantially [as the proper threshold voltage] equal, or has threshold voltage lower than it. Preferably, the control reading electrical potential difference impressed to the control line 74 is lower than the threshold voltage of the channel field part under the control gate 446, when the bit cel 440 is programmed, and when the bit cel 440 is eliminated, it is higher than the threshold voltage of the channel field part under the control gate 446. Therefore, the current which the channel field of the bit cel 440 is non-conductive, and flows that in case data are read in the programmed bit cel 440 is about 2microA. It is as small as the following. The detection amplifier (not shown) combined with a bit line 84 detects this small current, and the 1st logical value 1, for example, logic, is read in the bit cel 440. The current which the channel field of the bit cel 440 has conductivity, and flows that on the other hand in case data are read in the eliminated bit cel 440 is about 10microA. It is as large as the above. The detection amplifier (not shown) combined with a bit line 84 detects this high current, and reads the 2nd logical value and logic 0 in the bit cel 440.

[0042] The source 432,442 is in electrical-potential-difference RUREBERU respectively lower than a drain 434,444 between the processes which read data in the bit cel 430,440. The voltage drop of the channel field partial ends under the control gate 436,446 is small. The probability for a charge carrier to be accidentally poured in into a charge trap site from a channel field in this way is small. Furthermore, the channel field which separates a drain from the charge trap site in the 1st, the 2nd, and the bit cel of the 3rd line is turned off with the 2nd selection reading electrical potential difference impressed to the selection lines 61, 62, and 63. For this reason, the active jamming over the reading process of the 1st, the 2nd, and the bit cel of the 3rd line is small. Therefore, the reading process of this invention has reading disturbance smaller than the reading process by the conventional technique. Furthermore, NVM Since the bit line of equipment 50 is separated from the charge trap site in a bit cel by the selector gate in a corresponding bit cel, its capacity value of a parasitism bit line capacitor is substantially unrelated to the charge of a charge trap site. In other words, the data dependency of parasitism bit line capacity is NVM. In equipment 50, it is small. NVM NVM with the small data dependencies of bit line capacity, such as equipment 50, Equipment fits a high performance application.

[0043] as mentioned above, NVM Equipment and its NVM that the approach of accessing equipment was offered should understand -- it needs. Book NVM Equipment is a split gate FET. It has an array and is each FET. It has the control gate which exists in the top for channel field near the source part I, and the selector gate which exists in the top

for channel field near a drain part II. It can form as a side-attachment-wall spacer which **** to a selector gate, and, thereby, the control gate is NVM. The silicon area effectiveness of equipment is raised.

[0044] NVM FET of equipment In case it programs, it is accelerated in the channel field part between a selector gate and the control gate, and the charge carrier of the 1st polarity, for example, an electron, is poured in after that into the charge trap site located in the dielectric laminating circles which exist under the control gate. A selector gate controls the current which flows a channel field between programming processes. A programming process can be optimized about time effectiveness and the effectiveness of power.

[0045] NVM FET of equipment It is eliminated by pouring in the charge carrier of the 2nd polarity, for example, an electron hole, into a charge trap site from a channel field. Since a charge carrier penetrates the up dielectric layer of dielectric laminating circles and does not move between elimination processes, it uses a thick up dielectric layer, and it is NVM. The rate of data-hold of equipment can be raised.

[0046] NVM FET of equipment from -- in case data are read, a reading electrical potential difference is impressed to the drain which adjoins a selector gate. Therefore, reading disturbance and FET of data Destruction is suppressed to the minimum and, thereby, it is NVM further. The data-hold and dependability of equipment are improved. moreover, FET detecting the current which flows the bit line combined with a drain -- FET from -- data are read. FET A drain is separated from a charge trap site by the channel field part under a selector gate. In this way, the data dependency of bit line capacity is suppressed to the minimum, and it is NVM. Equipment fits a high performance application.

[Translation done.]

* NOTICES *

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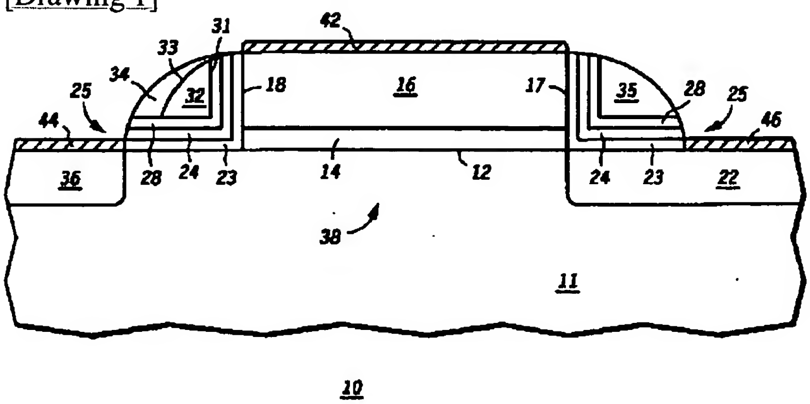
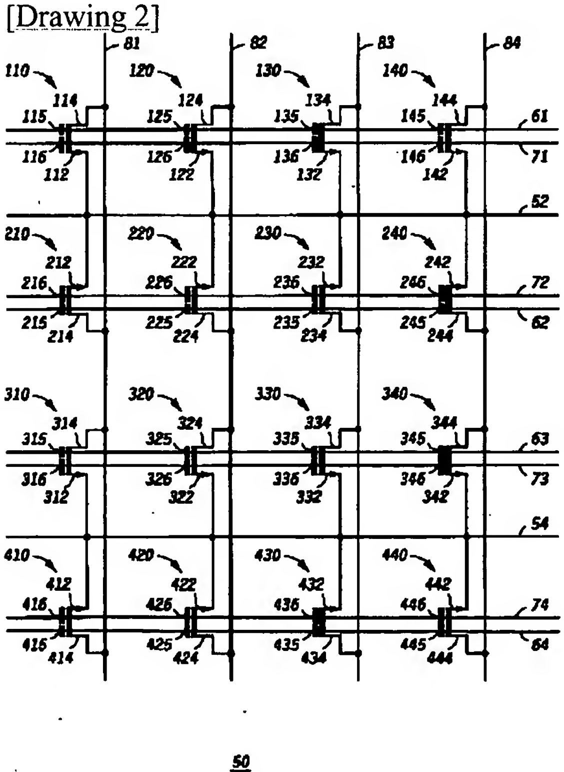
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



[Translation done.]